

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated December 27, 2007, has been received and its contents carefully reviewed.

Claims 1-14 are rejected by the Examiner. With this response, claims 1, 7, and 13 are amended. No new matter has been added. Claims 1-14 remain pending in this application.

In the Office Action, claims 1, 3, 4, and 6-14 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,535,194 to Hanano (hereinafter "Hanano"). Claims 2 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hanano in view of U.S. Patent No. 4,097,128 to Matsumoto (hereinafter "Matsumoto").

The rejection of claims 1, 3, 4, and 6-14 is respectfully traversed and reconsideration is requested.

Claims 1, 3, 4, and 6-12 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, "a light shutter on the liquid crystal display panel operable to transmit and shut off a light emitted from the liquid crystal display panel during every field period" and "wherein every field period is initiated upon a first transition of a gate signal from a low voltage signal to a high voltage signal to apply image data to the pixel and is terminated upon a next transition of the gate signal from a low voltage signal to a high voltage signal to apply image data to the pixel, and the light shutter is opened at a first transition of the gate signal and closed after the first transition of the gate signal and before the next transition of the gate signal per every frame period." Hanano does not teach or suggest at least this feature of the claimed invention.

In the Office Action the Examiner refers to Fig. 5a as teaching Even and Odd halves make up a single frame image. Hanano teaches generating a field synchronizing signal (FIG. 4c) according to the synchronizing signal (corresponding to the gate signal); delaying the field synchronizing signal by times τ_1 and τ_2 , respectively (FIGs. 4d and 4e); and generating a TN shutter drive signal (FIG. 4f) according to the first field synchronizing signal delayed by time τ_1 (FIG. 4d) and the second field synchronizing signal delayed by time τ_2 (FIG. 4e). In Hanano, the light shutter is opened at a transition of the delayed first field synchronizing signal from a low voltage signal to a high voltage signal and closed at a transition of the delayed second field synchronizing signal from a low voltage signal to a high voltage signal. Therefore, Hanano does

not teach these features of claims 1, 3, 4, and 6-12. Accordingly, Applicant submits that claims 1, 3, 4, and 6-12 are allowable over Hanano for at least this reason.

Claims 13 and 14 are allowable over the cited references in that each of these claims recites a method of driving a liquid crystal display, having a combination of features including, for example, "opening the light shutter a first transition of the gate signal from a low voltage signal to a high voltage signal; and closing the light shutter after the first transition of the gate signal and before a next transition of the gate signal from a low voltage signal to a high voltage signal per every frame period." In the Office Action, the Examiner rejects claim 13 using the same rationale given for claim 1. Applicant's submits that Hanano does not teach or suggest at least the above identified features of claims 13 and 14 for at least the reasons given above for claim 1. Accordingly, Applicant submits that claims 13 and 14 are allowable over Hanano.

The rejection of claims 2 and 5 is respectfully traversed. As discussed above with respect to claims 1, 3, 4, and 6-14, Hanano fails to teach the features discussed above. Matsumoto fails to cure this deficiency of Hanano. Accordingly, Applicant submits that claims 2 and 5 are allowable over Hanano and Matsumoto.

Applicants believe the application is now in condition for allowance and early, favorable action is respectfully solicited. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911.

Application No. 10/015,679
Amendment dated March 19, 2008
Response to Office Action dated December 27, 2007

Docket No. 8734.037 US

Please credit any overpayment to deposit Account No. 50-0911.

Dated: March 19, 2008

Respectfully submitted,

By Valerie P. Hayes

Valerie P. Hayes

Registration No.: 53,005

McKENNA LONG & ALDRIDGE LLP

1900 K Street, N.W.

Washington, DC 20006

(202) 496-7500

Attorneys for Applicant